Microcontroller power management AN0302

PLC18V8Z APPLICATIONS

The 80C51 microcontroller and its CMOS derivatives have two power reducing modes, Idle and Power Down. The Power Down mode reduces the device's current to less than 50µA by only keeping the on-chip RAM and SFRs data intact. In order to resume operation while in the Power Down mode, it is necessary to apply a reset to the microcontroller.

The PLC18V8Z is in a low power mode whenever its inputs are not switching, drawing less than 100µA. An input transition causes the PLC18V8Z to power up its internal array for a short time, latch a valid output and then return to low power mode. Because of this transparent power reduction feature and its programmability, the PLC18V8Z is an excellent device to use in low power applications with an 80C51 microcontroller.

Two examples of using the PLC18V8Z with a SC87C751 microcontroller are presented. Both applications use the PLC18V8Z to detect events while the SC87C751 is in a Power Down mode and then reset (wake up) the microcontroller. The first example, shown in Figure 1, uses the PLC18V8Z as an 8-bit priority encoder. SNAP pin layout and listing of the circuitry fused inside the PLC18V8Z is shown in Figure 2.

Whenever one of the inputs $I_7 – I_0$ goes LOW, a binary representation of its position is output on pins $A_3 – A_0$. If more than one input is Active-LOW, then the input with the highest priority is represented on the output, where I_7 has the highest priority. Another output, $\overline{EO}$, is not connected to the microcontroller but is used to control the RST output of the PLC18V8Z. $\overline{EO}$ is Active-LOW anytime all inputs are high. Actually, the PLC18V8Z could easily be reprogrammed to output the inverse of this signal which could be tied to the interrupt line of the microcontroller to generate an interrupt anytime one or more inputs were low.

Pin 16 of the PLC18V8Z, labeled RST, is the output of a 3-State buffer whose input is always high. The buffer's control line is tied internally to a product term which is enabled by $\overline{EO}$ and an input from the microcontroller labeled $\overline{RSTEN}$. The RST buffer may be in only two states, either driving a high (resetting the SC87C751) or 3-State (allowing C_3 to discharge), enabling normal operation of the microcontroller. Before entering the Power Down mode, the microcontroller should force $\overline{RSTEN}$ low. Then, any low on $I_7 – I_0$ will cause $\overline{EO}$ and also RST high, resetting the microcontroller. When the microcontroller is reset, it will force its ports to input mode and since P_1 and P_3 have internal pull-up resistors, $\overline{RSTEN}$ will go high forcing RST into the 3-State mode allowing C_3 to discharge.

The second example, shown in Figure 3, with SNAP pin layout and listing in Figure 4, uses the PLC18V8Z to monitor three microcontroller input lines ($I_{NC} – I_{NA}$) and reset the microcontroller upon any change. Three internal registers inside the PLC18V8Z are used to hold the states or levels of the input lines prior to entering Power Down mode. Before entering Power Down mode, the microcontroller should clock into the PLC18V8Z the states of $I_{NC} – I_{NA}$ with the LOAD signal. Comparator logic fused into the PLC18V8Z compares the output of the registers to the three input lines. The RST output of the PLC18V8Z operates in a similar manner to the first example to reset the microcontroller whenever $\overline{RSTEN}$ is low and the output of the comparator is false.

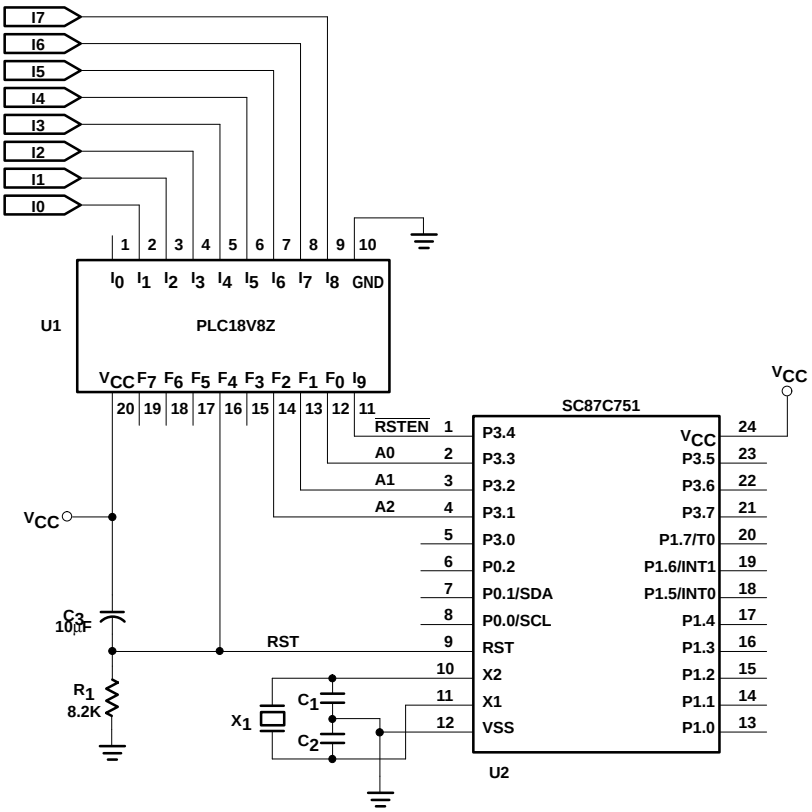

Figure 1.

```
*********************************************************
*       PLC18V8Z 20-Pin DIP Package Pin Layout          *
* Date: 10/03/93                        Time: 15:27:18 *
*********************************************************

                  _________   _________
                 |         \_____/         |
                 |                         |
              [ 1|I0/CLK               VCC|20]
         I0 [ 2|I1                     F7|19]
         I1 [ 3|I2                     F6|18]
         I2 [ 4|I3                     F5|17]
         I3 [ 5|I4                     F4|16] RST
         I4 [ 6|I5                     F3|15] EO
         I5 [ 7|I6                     F2|14] A2
         I6 [ 8|I7                     F1|13] A1
         I7 [ 9|I8                     F0|12] A0
              [10|GND               I9/OE_|11] RSTEN
                 |                         |
                 |_________________________|
```

```
@PINLIST
I0 i;I1 i;I2 i;I3 i;
I4 i;I5 i;I6 i;I7 i;
RSTEN i;
A0 o;A1 o;A2 o;
EO o;RST o;

@GROUPS
@TRUTHTABLE
@LOGIC EQUATIONS

A0   =  /I1*I2*I3*I4*I5*I6*I7
      +      /I3*I4*I5*I6*I7
      +            /I5*I6*I7
      +                  /I7;
A1   =     /I2*I3*I4*I5*I6*I7
      +      /I3*I4*I5*I6*I7
      +               /I6*I7
      +                  /I7 ;
A2   =           /I4*I5*I6*I7
      +            /I5*I6*I7
      +               /I6*I7
      +                  /I7 ;
EO  =  /(I0*I1*I2*I3*I4*I5*I6*I7);
RST  =  1;
RST.OE = /RSTEN*EO;

@INPUT VECTORS
@OUTPUT VECTORS
@STATE VECTORS
@TRANSITIONS
```

Figure 2.

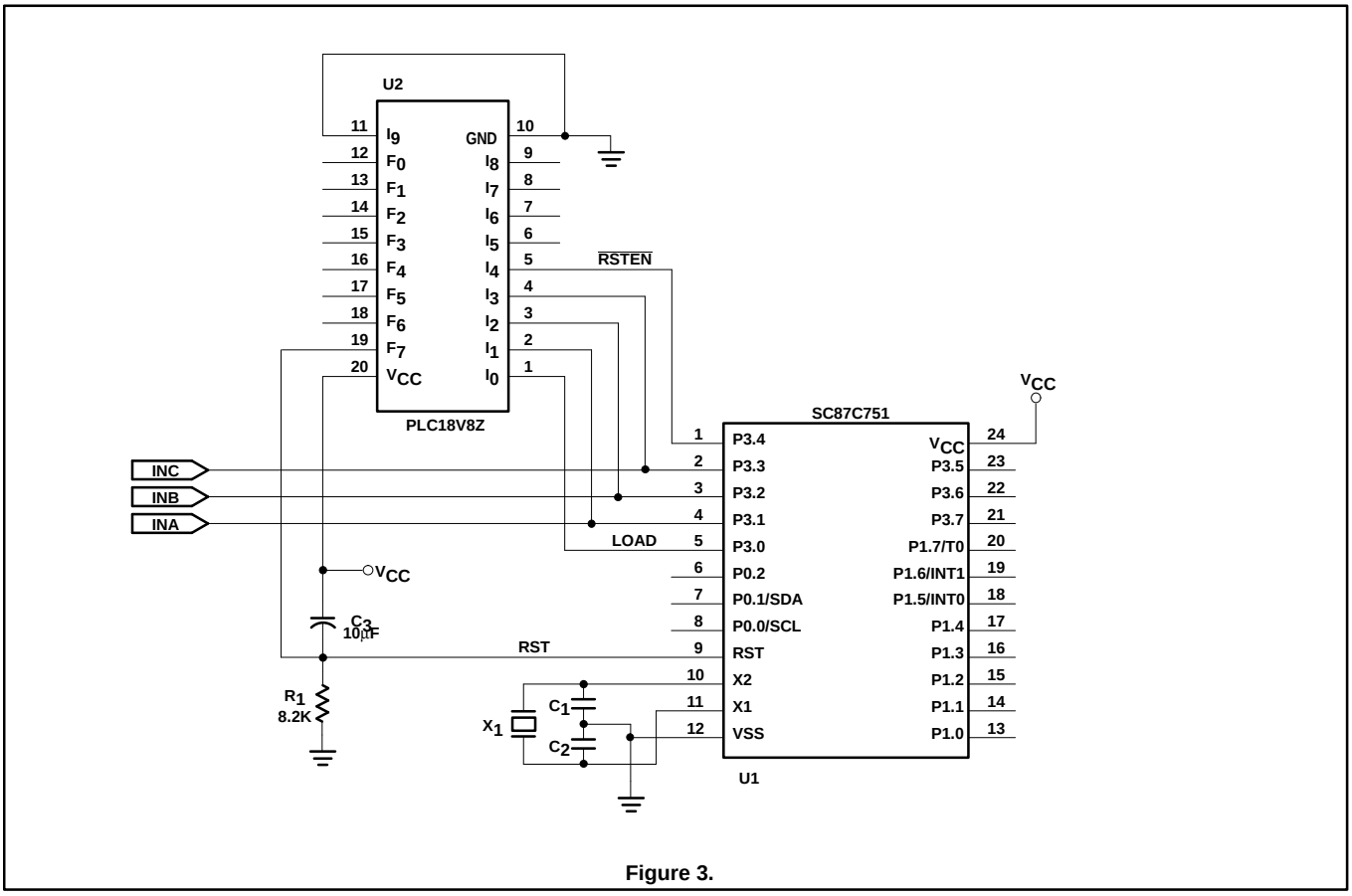
U2
PLC18V8Z
SC87C751
U1
RSTEN
LOAD
RST
INC
INB
INA
VCC
R1
8.2K
C3
10µF
X1
C1
C2

Figure 3.

```
************************************************************
*       PLC18V8Z 20-Pin DIP Package Pin Layout             *
* Date: 10/03/93                            Time: 15:27:00 *
************************************************************

                    _________   _________
                   |         \_____/         |
                   |                         |
            LOAD [ 1|I0/CLK                VCC|20]
             INA [ 2|I1                     F7|19] RST
             INB [ 3|I2                     F6|18] OUTC
             INC [ 4|I3                     F5|17] OUTB
           RSTEN [ 5|I4                     F4|16] OUTA
                 [ 6|I5                     F3|15] COMP
                 [ 7|I6                     F2|14] NDC
                 [ 8|I7                     F1|13] NDB
                 [ 9|I8                     F0|12] NDA
                 [10|GND                I9/OE_|11] OEN
                    |                         |
                    |_________________________|
```

```
@PINLIST

LOAD  i;INA   i;INB   i;
INC   i;RSTEN i;OEN   i;

OUTA  o;OUTB  o;OUTC  o;
COMP  o;NDA   o;NDB   o;
NDC   o;RST   o;

@GROUPS
@TRUTHTABLE
@LOGIC EQUATIONS

da.d   = ina;   "flip-flop equation"
da.clk = load;
nda = /da;      "invert buffer to pin equa-
tion"
nda.oe = /oen;

db.d   = inb;
db.clk = load;
ndb = /db;
ndb.oe = /oen;

dc.d   = inc;
dc.clk = load;
ndc = /dc;
ndc.oe = /oen;

outa = da*ina + /da*/ina;  "comparator"
outb = db*inb + /db*/inb;
outc = dc*inc + /dc*/inc;
comp = outa * outb * outc;

rst =  1;                  "3-state reset
control"
rst.oe = /rsten * /comp;   "enable when
rsten is low and no compare"

@INPUT VECTORS
@OUTPUT VECTORS
@STATE VECTORS
@TRANSITIONS
```

Figure 4.